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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,728	09/26/2003	Hironobu Kariyazono	59520 (48229)	9422

21874 7590 02/28/2006

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

N.A

Office Action Summary	Application No.	Applicant(s)	
	10/672,728	KARIYAZONO, HIRONOBU	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,17 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,17 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the RCE filed 6 December 2005.

Drawings

The drawings were received on 26 September 2003. These drawings are acceptable.

Information Disclosure Statement

The information disclosure statement filed 6 December 2005 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (U.S. Patent 5,618,749) in view of Morris et al. (U.S. Patent 4,830,976).

In re claims 13 and 34, Takahashi discloses a field effect transistor (Figs. 11 and 12) that contains a semiconductor layer (100); an MOS transistor (50) formed on the semiconductor layer; a resistive conductive layer (R/2) formed on the semiconductor layer, a silicon nitride layer or a silicon oxynitride layer (1) (protective layer (claim 34)), (Column 6, lines 35-44) formed on the resistive conductive layer; and a silicon oxide layer (8) formed on the side of the resistive layer, since layer (8) is formed of an insulating film and that is a dielectric layer as described it can be formed of silicon oxide. (Column 9, lines 1-4, column 6, lines 35-36) Takahashi discloses all the limitations except for the resistive conductive layer to have a center part and two ends. Whereas Morris discloses a field effect transistor (Figs. 7 and 9) that contains a resistor having a center part (W area) and two ends (areas with the contact window), where the width of the two ends are wider than a width of the center part. The resistor has a center part and two ends for placement and connection of the contacts of the device. (Column 7, lines 29-30, Fig. 7) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Takahashi by incorporating the resistive conductor layer to have a center part and two ends for placement and connection of the contacts of the device as taught by Morris.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi and Morris as applied to claim 13 above, and further in view of Kanda et al. (U.S. Publication 2003/0034531).

In re claim 17, Takahashi and Morris disclose all the limitations except for a high and low breakdown voltage transistor. Whereas Kanda discloses a semiconductor device (Fig. 28) that contains a MOS high voltage breakdown transistor (HV) and a low voltage breakdown transistor (LV) of insulated gate types formed on a semiconductor layer (100), where the high voltage transistor includes a proof voltage between a source and drain, which is different from the low breakdown voltage transistor. The high and low breakdown voltage transistors are formed so the high voltage act as an actuation output module to have a high withstanding breakdown voltage and the low voltage transistor to act as a logic module for controlling the actuation output module. (Page 1, Paragraph 0004) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Takahashi and Morris by incorporating a high and low breakdown voltage transistors so the high voltage act as an actuation output module to have a high withstanding breakdown voltage and the low voltage transistor to act as a logic module for controlling the actuation output module as taught by Kanda.

Response to Arguments

Applicant's arguments with respect to claims 13,17 and 34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on T-F 8:30-6:00 off Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR